Saw Xue Zheng

Phone: + 420 774 952 477
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Repositories: github.com/saw235

Education

Pennsylvania State University **Class of 2017**
Bachelor of Science in Electrical Engineering **GPA - 3.51**
Minor in Computer Science

University Science Malaysia **Class of 2019**
Master of Science in Electrical System Design Engineering **GPA - 3.56**
MSc Thesis: Achieving Pitch Control in Fixed Wing Aircraft Through Moving Mass Control System

Skills

- Proficient programming skills in C/C++ (4+ years), Python (5+), Javascript/AJAX (4+), C# (1+) and others
- Experience in utilizing Software Engineering paradigms such as git version control, OOP, and Design Patterns
- Experience in implementing machine learning algorithms
- Experience in working with relational databases such as Sybase SQL, MSSQL, and SQLite
- PowerShell, Bash, Awk and Perl scripting for task automation and text processing

- Experience in working with MATLAB and Jupyter
- Experience in working with data massaging/visualization tools like Matplotlib and Numpy.
- Experience in working with different microcontrollers and peripherals/modules such as DC motors, servos, temperature sensor, and capacitive touchscreen.
- .Relevant lab experiences in using oscilloscopes, logic analyzer, and spectrum analyzer

- Experience in ASIC/FPGA digital hardware design using both VHDL and SystemVerilog
- Experience in test bench writing and verification methodologies such as OVM and UVM
- Knowledge of ACPI standard
- Experience in RISC-V ecosystem and toolchain

- Ability to self-learn a topic and manage a project
- Ability to create good documentations of my own work

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Work Experiences

Codasip **Brno, Czech Republic**
Field Application Engineer **Oct 2020**
- Assist and provide technical answers to clients
- Ported ThreadX RTOS for the RISC-V gnu toolchain

Codasip **Brno, Czech Republic**
Computer Hardware Engineer **May 2019**
- Processor pipeline design and optimization.
- Worked with instruction decoder, branch prediction implementations, pipeline retiming and return address stack
- Developed synthesis flow and provide timing closure for core IPs through Cadence/Mentor/Synopsys synthesis and LEC tools.
- Design and improve existing testbench for verification.
- Worked on D and B (Double and Bitmanip) RISC-V extensions in Berkelium Cores.
- Worked on bringing up the SweRV Support Package team, providing technical and EDA tooling support to SweRV EH1, EH2, and EL2 Cores by Western Digital.
- Experience in FuseSoC and Edalize, the open source HDL packaging system.

Intel **Penang, Malaysia**
Pre-Silicon Verification Engineer **Jan 2018**
- Front-end (RTL) validation and verification of Power Management Controller and Power Gating Controller Block
- Improved scalability, maintainability and reduced total compile/elaboration time for System Verilog test benches
- Ensured reliability of IP by enabling and performing Lint and CDC checks
- Ensure manufacturing testability by utilizing the DFT methodologies
- Ensured high-quality delivery and release of IP by performing FPV through JasperGold software.

Technical Graduate Trainee **August 2017**
- Developed external and internal tools, web services, and applications for test data management
- Reduced data process turnaround time by automating backend data process

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Pre-Silicon Verification Intern **Summer 2015**

• Front-end (RTL) validation and verification of Intel Chipset USB IP

• Ensured that IP are sufficiently tested by exercising test coverage methodology

Penn State Learning Resource Center **Behrend, PA**

Peer Tutor **Spring 2014 - Spring 2017**

• Tutored peers in Mathematics, Electrical and Computer Science subjects by appointments or walk-ins

• Nominated for Outstanding Tutor Award

Relevant Coursework Taken

• Embedded System Design
• Signals and System
• Artificial Intelligence
• Control Systems
• Advanced Analog Integrated Circuit Design
• Advanced Digital Design
• Circuits and Electronics I/II
• Net-centric Computing
• Energy Conversion
• Signal Integrity for High-Speed Digital Design

Projects

• ***Capacitive Sensing CPAP mask*** Spring 2017

• ***Real-time image processing with FPGA*****,** implemented using a Nexys 4-DDR board Fall 2016

• ***Achieving Pitch Control in Fixed Wing Aircraft Through Moving Mass Control System*** Fall 2018